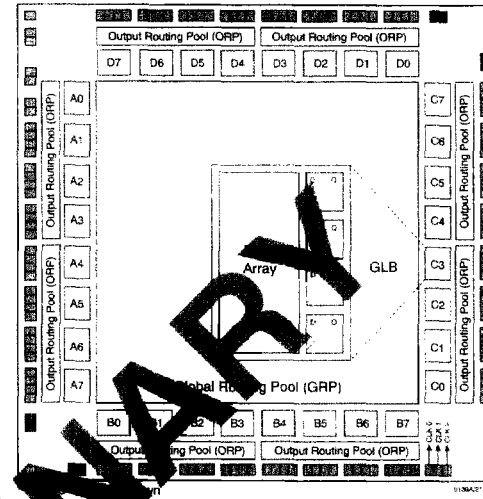
ispLSI® 2128VE

3.3V In-System Programmable SuperFAST™ High Density PLD

Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **6000 PLD Gates**
  - **128 and 64 I/O Pin Versions, Eight Dedicated Inputs**
  - **128 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **100% Functional/JEDEC Upward Compatible with ispLSI 2128V Devices**
- **3.3V LOW VOLTAGE 2128 ARCHITECTURE**
  - **Interfaces with Standard 5V TTL Devices**
  - **128 I/O Pin Version is Fuse Map Compatible with 5V ispLSI® 2128 and 2128E**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **f_{max} = 180 MHz Maximum Operating Frequency**
  - **t_{pd} = 5.0 ns Propagation Delay**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **3.3V In-System Programmability (ISP™) Using Boundary Scan Test Access Port (TAP)**
  - **Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR Bus Arbitration Logic**
  - **Increased Manufacturing Yields, Reduced Time-To-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **Superior Quality of Results**
  - **Tightly Integrated with Leading CAE Vendor Tools**
  - **Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **PC and UNIX Platforms**

Functional Block Diagram*



Description

The ispLSI 2128VE is a High Density Programmable Logic Device available in 128 and 64 I/O-pin versions. The device contains 128 Registers, eight Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2128VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2128VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2128VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see Figure 1). There are a total of 32 GLBs in the ispLSI 2128VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

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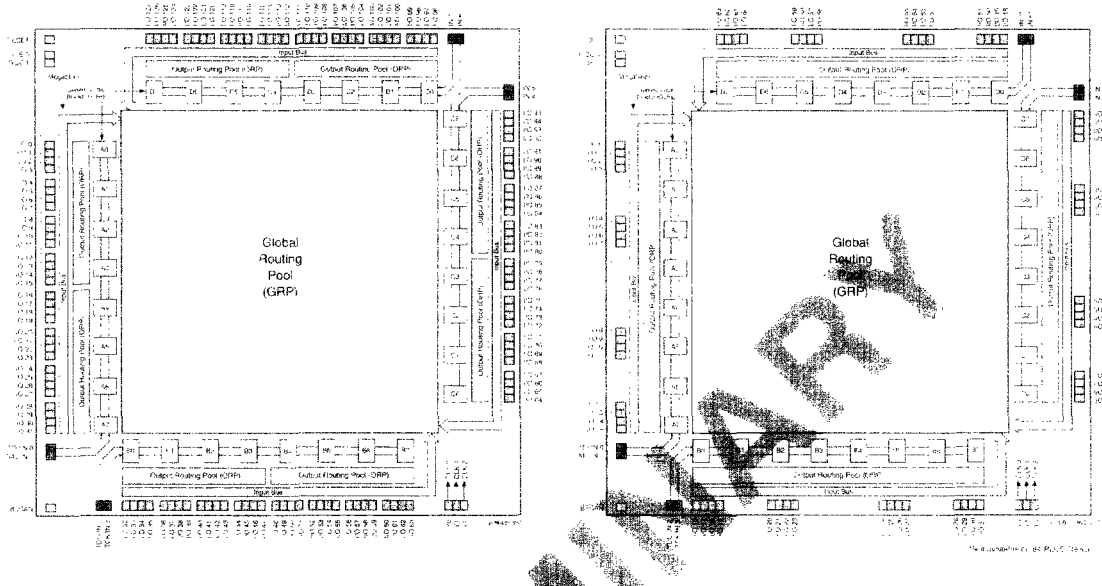
Functional Block Diagram

Figure 1. ispLSI 2128VE Functional Block Diagram (128-I/O and 64-I/O Versions)



The 128-I/O 2128VE contains 128 I/O cells, while the 64-I/O version contains 64 I/O cells. Each I/O cell is directly connected to an I/O pin and can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4mA or sink 8mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5V signal levels to support mixed-voltage systems.

Eight GLBs, 32 or 16 I/O cells, two dedicated inputs and two or one ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 or 16 universal I/O cells by the two or one ORPs. Each ispLSI 2128VE device contains four Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2128VE device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2128VE are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. When this fuse is erased (JEDEC "1"), the output is configured as a totem-pole output. When this fuse is programmed (JEDEC "0"), the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispEXPERT software tools.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[4] COND.	#[2]	DESCRIPTION[1]	-180		-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	5.0	–	7.5	–	10.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	7.5	–	10.0	–	13.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	180	–	135	–	100	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $(\frac{1}{t_{su2} + t_{co1}})$	118	–	100	–	77	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	200	–	143	–	100	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	4.0	–	5.0	–	6.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	3.5	–	[illegible]	–	5.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	[illegible]	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	5.0	[illegible]	[illegible].0	–	[illegible].0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	[illegible].5	[illegible]	5.0	–	6.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	[illegible]	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	[illegible]	7.0	[illegible]	10.0	–	13.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	[illegible].0	[illegible]	5.0	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	[illegible]	10.0	–	12.0	–	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	[illegible]	10.0	–	12.0	–	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	5.0	–	7.0	–	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	5.0	–	7.0	–	9.0	ns
t_{wh}	–	18	External Synchronous Clock Pul[illegible]ation, High	2.5	–	3.5	–	5.0	–	ns
t_{wl}	–	19	External Synchronous Cl[illegible]se Duration, Low	2.5	–	3.5	–	5.0	–	ns

Table 2-0030/2128VE

1. Unless noted otherwise, all parameters use the GR[illegible]20 P[illegible]OR[illegible]th, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further de[illegible]s.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions secti[illegible]